Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Previously Presented) A power-on reset circuit, comprising:

a Schmitt trigger circuit comprising a plurality of MOS devices and a threshold-enhancement node, each of said devices having the same V_t for determining a power reset trigger level, the threshold-enhancement node having a first voltage when the Schmitt trigger circuit is in a power-down mode and having a second voltage when the Schmitt trigger circuit is in a sleep mode; and

a voltage divider connected to an input of the Schmitt-trigger circuit and configured to track a supply signal.

2. (Currently Amended) The power-on reset circuit according to claim 1, and further comprising a compensate circuit operatively coupled to the Schmitt trigger circuit for generating a reset pulse to compensate for temperature and a supply signal variation effect.

3. (Previously Presented) The power-on reset circuit according to claim 1, wherein the voltage divider includes a current source transistor operative to generate a current in response to the supply signal.

4. (Previously Presented) The power-on reset circuit according to claim 1, wherein the voltage divider includes a low-side resistor for reduction of leakage current.

5. (Original) The power-on reset circuit according to claim 1, wherein the voltage divider includes a compensate circuit operative to adjust a feedback current to restore a voltage at the input of the Schmitt-trigger circuit, in response to a fluctuation in the supply signal.

6. (Previously Presented) The power-on reset circuit according to claim 1, wherein the first voltage is greater than zero and the second voltage is less than the first voltage.

7. (Currently Amended) The power-on reset circuit according to claim 1, wherein the Schmitt trigger circuit further comprises a reset signal node operative to rise from a ground potential to a first ~~voltage~~ potential in response to an increase of the supply signal when the supply signal has compared favorably to a first threshold ~~voltage~~ potential, and to drop from the first voltage to the ground potential when the supply signal has not compared favorably to the first threshold voltage, if the Schmitt trigger circuit has not entered the sleep mode.

8. (Previously Presented) The power-on reset circuit according to claim 1, wherein the Schmitt trigger circuit further comprises a reset signal node having a first voltage peak when the Schmitt trigger circuit enters the power-down mode and having a second voltage peak, which is greater than the first voltage peak, when the Schmitt trigger circuit exits the power-down mode.

9. (Previously Presented) The power-on reset circuit according to claim 8, wherein the reset signal node further has a third voltage when the Schmitt trigger circuit enters and exits the sleep mode and wherein the third voltage is less than the first voltage peak.

10. (Previously Presented) A method for providing a reset signal in response to a supply signal, the method comprising:

generating a primary current in response to the supply signal;

generating a trigger voltage in response to the primary current;

if a sleep mode has not been entered and the supply signal has not compared favorably to a first threshold level, increasing the reset signal from a reference potential to a first potential in response to an increase in the supply signal; and

if the sleep mode has been entered and the supply signal has compared favorably to the first threshold level, setting the reset signal to the reference potential;

wherein the reset signal is increased from the reference potential to the first potential in response to the increase in the supply signal when a power-up state is entered and is increased

from the reference potential to a second potential in response to a decrease in the supply signal when a power-down state is entered, the first potential being greater than the second potential.

11. Cancelled.

12. (Previously Presented) The method for providing a reset signal in response to a supply signal of claim 10, further comprising compensating the trigger voltage in response to a change in temperature, wherein the compensating of the trigger voltage in response to a change in temperature includes:

providing a primary current path having a path current corresponding to the primary current and the trigger voltage; and

in a circuit having a complementary temperature coefficient with respect to a current source for generating the primary current, adjusting the path current of the primary current path to compensate the path current for temperature-dependent current variations.

13. (Previously Presented) The method for providing a reset signal in response to a supply signal of claim 12, wherein the adjusting of the path current of the primary current path to compensate the path current for temperature-dependent current variations includes:

providing a compensation path in parallel to a low-end portion of the primary current path; and

increasing a compensation current in the compensation path in response to a decrease in the primary current, and

decreasing the compensation current in the compensation path in response to an increase in the primary current.

14. (Previously Presented) A computer system comprising:

a microprocessor;

a bus coupled to the microprocessor;

a memory coupled to the bus; and

the power-on reset circuit of claim 1 operative to generate a power-on reset signal to the microprocessor.

15. (Previously Presented) The computer system of claim 14, wherein the power-on reset circuit further comprises a compensate circuit operatively coupled to the Schmitt trigger circuit for generating a reset pulse to compensate for temperature and a supply signal variation effect.

16. (Previously Presented) The computer system of claim 14, wherein the voltage divider includes a current source transistor operative to generate a current in response to the supply signal.

17. (Previously Presented) The computer system of claim 14, wherein the voltage divider includes a low-side resistor for reduction of leakage current.

18. (Original) The computer system of claim 14, wherein the voltage divider includes a compensate circuit operative to adjust a feedback current to restore a voltage at the input of the Schmitt-trigger circuit, in response to a fluctuation in temperature.

19. (Previously Presented) The computer system of claim 14, wherein the Schmitt trigger circuit further comprises a reset signal node operative to rise from a ground potential to a first potential in response to an increase of the supply signal when the supply signal has compared favorably to a first threshold voltage, and to drop from the first potential to the ground potential when the supply signal has not compared favorably to the first threshold voltage, if the Schmitt trigger circuit has not entered the sleep mode.

20. (Previously Presented) The computer system of claim 14, wherein the Schmitt trigger circuit further comprises a reset signal node operative to rise from a ground potential to a first potential in response to a change of the supply signal during either a power-up or power-down mode but not during an entering or exiting of the sleep mode.

21. (Currently Amended) The computer system of claim 20, wherein:

the ~~Schmitt trigger circuit further comprises a~~ reset signal node is operative to rise from the ground potential to the first potential in response to a change of the supply signal during ~~a~~ the power-up mode and to rise from the ground potential to a second potential in response to ~~a~~ another change of the supply signal during the power-down mode; and

the first potential is greater than the second potential.

22. (Currently Amended) The computer system of claim 14, wherein:

the Schmitt trigger circuit further comprises a reset signal node ~~is~~ operative to rise from a ground potential to a first potential in response to a change of the supply signal during a power-up mode and to rise from a ground potential to a second potential in response to ~~a~~ another change of the supply signal during a power-down mode; and

the first potential is greater than the second potential.

23. (Previously Presented) A method for providing a reset signal in response to a supply signal, the method comprising:

generating a primary current in response to the supply signal;

generating a trigger voltage in response to the primary current;

if a sleep mode has not been entered and the supply signal has not compared favorably to a first threshold level, increasing the reset signal from a reference potential to a first potential in response to an increase in the supply signal; and

if the sleep mode has not been entered and the supply signal has compared favorably to the first threshold level, setting the reset signal to the reference potential;

wherein the reset signal is increased from the reference potential to the first potential in response to the increase in the supply signal when a power-up state is entered, the reset signal is increased from the reference potential to a second potential in response to a decrease in the supply signal when a power-down state is entered, and the first potential is greater than the second potential.

24. (Previously Presented) The method for providing a reset signal in response to a supply signal of claim 23, further comprising compensating the trigger voltage in response to a change in temperature, wherein the compensating of the trigger voltage in response to a change in temperature includes:

providing a primary current path having a path current corresponding to the primary current and the trigger voltage; and

in a circuit having a complementary temperature coefficient with respect to a current source, adjusting the path current of the primary current path to compensate the path current for temperature-dependent current variations.

25. (Previously Presented) The method for providing a reset signal in response to a supply signal of claim 24, wherein the adjusting of the path current of the primary current path to compensate the path current for temperature-dependent current variations includes:

providing a compensation path in parallel to a low-end portion of the primary current path; and

increasing a compensation current in the compensation path in response to a decrease in the primary current, and decreasing the compensation current in the compensation path in response to an increase in the primary current.

26. Cancelled.

27. (Currently Amended) A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; and

a voltage divider connected to an input, and not controlled by an output, of the Schmitt-trigger circuit and configured to track a supply signal, the voltage divider comprising resistors connected directly to the Schmitt trigger circuit; and

a compensate circuit operatively coupled to the Schmitt trigger circuit for generating a reset pulse to compensate for temperature and a supply signal variation effect.

28. (Currently Amended) A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; and

a voltage divider connected to an input, and not controlled by an output, of the Schmitt-trigger circuit and configured to track a supply signal, the voltage divider comprising resistors connected directly to the Schmitt trigger circuit, wherein the voltage divider further includes a current source transistor operative to generate a current in response to the supply signal.

29. (Previously Presented) The power-on reset circuit according to claim 28, wherein the resistors of the voltage divider include a low-side resistor for reduction of leakage current.

30. (Currently Amended) A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; and

a voltage divider connected to an input, and not controlled by an output, of the Schmitt-trigger circuit and configured to track a supply signal, the voltage divider comprising resistors connected directly to the Schmitt trigger circuit, wherein the voltage divider further includes a compensate circuit operative to adjust a feedback current to restore a voltage at the input of the Schmitt-trigger circuit, in response to a fluctuation in the supply signal.

31. (Previously Presented) The power-on reset circuit according to claim 30, wherein the Schmitt trigger circuit further comprises a threshold-enhancement node having a first voltage greater than zero when the Schmitt trigger circuit enters and exits a power-down mode and having a second voltage less than the first voltage when the Schmitt trigger circuit enters and exits a sleep mode.

32. (Currently Amended) The A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; and

a voltage divider connected to an input, and not controlled by an output, of the Schmitt-trigger circuit and configured to track a supply signal, the voltage divider comprising resistors connected directly to the Schmitt trigger circuit, wherein the Schmitt trigger circuit further comprises a reset signal node operative to rise from a ground potential to a first voltage in response to an increase of the supply signal when the supply signal has compared favorably to a first threshold voltage, and to drop from the first voltage to the ground potential when the supply signal has not compared favorably to the first threshold voltage, if the Schmitt trigger circuit has not entered a sleep mode.

33. (Currently Amended) A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; and

a voltage divider connected to an input, and not controlled by an output, of the Schmitt-trigger circuit and configured to track a supply signal, the voltage divider comprising resistors connected directly to the Schmitt trigger circuit, wherein the Schmitt trigger circuit further comprises a reset signal node having a first voltage peak when the Schmitt trigger circuit enters a power-down mode and having a second voltage peak, which is greater than the first voltage peak, when the Schmitt trigger circuit exits the power-down mode.

34. (Previously Presented) The power-on reset circuit according to claim 33, wherein the reset signal node further has a third voltage when the Schmitt trigger circuit enters and exits a sleep mode and wherein the third voltage is less than the first voltage peak.

35. (Currently Amended) A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; ~~and~~

a voltage divider connected to an input of the Schmitt-trigger circuit and configured to track a supply signal, and ~~further~~ comprising a compensate circuit operatively coupled to the Schmitt trigger circuit for generating a reset pulse to compensate for temperature and a supply signal variation effect; and

a node having a first potential corresponding to a power-down mode of the Schmitt trigger circuit and having a second potential corresponding to a sleep mode of the Schmitt trigger circuit.

36. (Currently Amended) A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; ~~and~~

a voltage divider connected to an input of the Schmitt-trigger circuit and configured to track a supply signal, wherein the voltage divider includes a current source transistor operative to generate a current in response to the supply signal; and

a node having a first potential corresponding to a power-down mode of the Schmitt trigger circuit and having a second potential corresponding to a sleep mode of the Schmitt trigger circuit.

37. (Currently Amended) A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; ~~and~~

a voltage divider connected to an input of the Schmitt-trigger circuit and configured to track a supply signal, wherein the voltage divider includes a compensate circuit operative to adjust a feedback current to restore a voltage at the input of the Schmitt-trigger circuit, in response to a fluctuation in the supply signal; and

a node having a first potential corresponding to a power-down mode of the Schmitt trigger circuit and having a second potential corresponding to a sleep mode of the Schmitt trigger circuit.

38. (Currently Amended) A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; ~~and~~

a voltage divider connected to an input of the Schmitt-trigger circuit and configured to track a supply signal, wherein the Schmitt trigger circuit further comprises a reset signal node

operative to rise from a ground potential to a first voltage in response to an increase of the supply signal when the supply signal has compared favorably to a first threshold voltage, and to drop from the first voltage to the ground potential when the supply signal has not compared favorably to the first threshold voltage, if the Schmitt trigger circuit has not entered a sleep mode; and

a node having a first potential corresponding to a power-down mode of the Schmitt trigger circuit and having a second potential corresponding to a sleep mode of the Schmitt trigger circuit.

39. (Currently Amended) A power-on reset circuit, comprising:

a Schmitt trigger circuit constructed with a plurality of MOS devices, each of said devices having the same V_t, for determining a power reset trigger level; ~~and~~

a voltage divider connected to an input of the Schmitt-trigger circuit and configured to track a supply signal,, wherein the Schmitt trigger circuit further comprises a reset signal node having a first voltage peak when the Schmitt trigger circuit enters a power-down mode and having a second voltage peak, which is greater than the first voltage peak, when the Schmitt trigger circuit exits the power-down mode; and

a node having a first potential corresponding to a power-down mode of the Schmitt trigger circuit and having a second potential corresponding to a sleep mode of the Schmitt trigger circuit.